CLAIMS

What is claimed is:

1. A method comprising, etching a metal silicide layer during fabrication of an integrated circuit in a Cl_2/O_2 environment having an O_2 concentration of greater than or equal to 25% by volume.

2. The method of claim 1 wherein the Cl_2/O_2 environment is provided at a pressure of approximately 2 - 40 mili-Torr.

3. The method of claim 2 wherein the pressure is approximately 3 mili-Torr.

4. The method of claim 1 wherein the Cl_2/O_2 environment is provided in a reactor with a source power of approximately 200 - 2000 Watts.

5. The method of claim 4 wherein the source power is approximately 400 Watts.

6. The method of claim 1 wherein the Cl_2/O_2 environment is provided in a reactor having a bias power of approximately 35 to 400 Watts.

7. The method of claim 6 wherein the reactor has a bias power of approximately 50 Watts.

8. The method of claim 1 wherein the metal silicide layer is a tungsten silicide layer.

9. The method of claim 1 wherein the Cl_2/O_2 environment comprises approximately 45 sccm Cl_2 and 30 sccm O_2.

10. The method of claim 9 wherein the Cl_2/O_2 environment is provided for a time period sufficient to completely etch the metal silicide layer.

11. The method of claim 9 wherein the time period is approximately 30 seconds.

12. A method comprising etching a metal silicide layer during fabrication of an integrated circuit in an environment having a high concentration of O_2 so as to fully etch the metal silicide layer without etching an underlying poly-silicon layer.

13. The method of claim 12 wherein the O_2 concentration is greater than or equal to 25% by volume.

14. The method of claim 12 wherein the environment comprises approximately 45 sccm Cl_2 and 30 sccm O_2.

15. The method of claim 12 wherein the metal silicide is chosen from the group consisting of tungsten silicide, chromium silicide and titanium silicide.

16. An integrated circuit comprising a metal silicide layer etched within an environment that provides high selectivity to poly-silicon.

17. The integrated circuit of claim 16 wherein the environment comprises a concentration of O_2 of at least 25% by volume.

18. The integrated circuit of claim 17 wherein the environment comprises a concentration of approximately 45 sccm Cl_2 and 30 sccm O_2.

19. The integrated circuit of claim 16 wherein the environment comprises a Cl_2/O_2 environment having a concentration of O_2 of at least 25% by volume.

20. The integrated circuit of claim 16 wherein the metal silicide layer comprises a portion of a gate structure.